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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,634	04/07/2005	Jurgen Holz	10808/231	7531

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EXAMINER	
CRUZ, LESLIE PILAR	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
08/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,634	HOLZ ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 May 2008 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US 2003/0107052 A1) in view of Chau et al. (US 5,908,313).

With respect to claim 9, Chan et al. (Figs. 1A-1I) discloses a field-effect transistor with local source-drain insulation, having a semiconductor substrate [100]; a source depression [106] and a drain depression [106], which are formed in a manner spaced apart from one another in the semiconductor substrate, wherein the source and drain depressions have, in an upper region, a widening with a predetermined depth for realizing defined channel connection regions [paragraph 0035]; a depression insulation

layer [110], which is formed at least in a bottom region of the source depression and of the drain depression, wherein the depression insulation layer has a depression sidewall insulation layer [110], which is formed in a sidewall region of the source and drain depressions but does not touch the gate dielectric [128]; and an electrically conductive filling layer [116], which is formed for realizing source [138] and drain [138] regions and for filling the source and drain depression at a surface of the depression insulation layer; a gate dielectric [128], which is formed at a substrate surface between the source and drain depressions; and a gate layer [126], which is formed at a surface of the gate dielectric, wherein the depression sidewall insulation layer extends into a region below the gate dielectric and overlaps with the gate and the gate dielectric. Chan et al. does not specify the electrically conductive filling layer has a seed layer for improving a deposition in the source and drain depressions, the seed layer comprising silicon or SiGe. However, Chau et al. (Fig. 3E) discloses it is well known for an electrically conductive filling layer [314] to have a seed layer, the seed layer comprising silicon [column 7 lines 33-46]. Chau et al. teaches the benefits of an electrically conductive filling layer having a seed layer, the seed layer comprising silicon, in order for the electrically conductive filling layer to be selectively deposited [column 7 lines 34-46]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the electrically conductive filling layer of Chan et al. to have a seed layer, the seed layer comprising silicon, such as taught by Chau et al., in order for the electrically conductive filling layer to be selectively deposited.

With respect to claim 5, Chan et al. in view of Chau et al. discloses the field-effect transistor as claimed in claim 9. Chan et al. (Figs. 1H-1I) further discloses a gate insulation layer [130] is formed at sidewalls of the gate layer.

With respect to claim 6, Chan et al. in view of Chau et al. discloses the field-effect transistor as claimed in claim 9. Chau et al. further discloses a field-effect transistor may be bounded by shallow trench isolations [column 4 lines 56-67]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the field effect transistor of Chan et al. in view of Chau et al. to be bounded by shallow trench isolations, such as taught by Chau et al., because of their ability to be formed to small dimensions with a high degree of planarity [Chau et al., column 4 lines 56-67].

With respect to claim 7, Chan et al. in view of Chau et al. discloses the field-effect transistor as claimed in claim 9. Chan et al. in view of Chau et al. does not disclose that the field-effect transistor has lateral structures < 100 nm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the field-effect transistor of Chan et al. in view of Chau et al. to have lateral structures < 100 nm in order to miniaturize the device while suppressing the resistance. The specific claimed relative dimensions of the lateral structures, absent any criticality, are only considered to be the “optimum” dimensions that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected

results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative thicknesses, it would have been obvious to one of ordinary skill in the art to use these values in the device of Chan et al. in view of Chau et al.

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, claim 7 is not patentably distinguishable over the Chan et al. in view of Chau et al. reference.

With respect to claim 8, Chan et al. in view of Chau et al. discloses the field-effect transistor as claimed in claim 9. Chan et al. further discloses the source and drain depressions have a depth of approximately 50 nm to 300 nm [paragraph 0019].

Response to Arguments

Applicant's arguments with respect to claim 9 have been considered but are moot in view of the new ground(s) of rejection.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leslie Pilar Cruz
Examiner
Art Unit 2826

/Minh-Loan T. Tran/
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